KSM50N50

500V N-Channel MOSFET

General Description

The KSM50N50 is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Product Summary

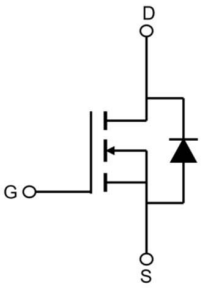
V_{DS} (V)	$R_{DS(on)}$ (mΩ)	I_D (A)
500	84 at V_{GS} = 10 V	50

Features

- Fast Switching
- LowON Resistance
- Low Gate Charge

TO-3PN Pin Configuration





Applications

- Power switch circuit of electron ballast and adaptor.

Absolute Maximum Ratings **Tc=25℃ unless otherwise noted**

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	±30	V
I_D	Drain Current – Continuous (T_C=25℃)	50	A
	Drain Current – Continuous (T_C=100℃)	28	A
I_{DM}	Drain Current – Pulsed[1]	140	A
P_D	Power Dissipation (T_C=25℃)	280	W
	Power Dissipation (T_C=100℃)	3.2	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	40	℃/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	0.5	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	500	---	---	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=500V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=400V , V_{GS}=0V , T_J=125℃	---	---	100	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±30V , V_{DS}=0V	---	---	±100	nA

On Characteristics

$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=15A	---	84	110	mΩ
		V_{GS}=4.5V , I_D=15A	---	98	130	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	2.0	3.1	4.0	V
gfs	Forward Transconductance	V_{DS}=15V , I_S=15A	---	35	---	S

Dynamic and switching Characteristics

Q_g	Total Gate Charge	V_{DS}=400V , V_{GS}=10V , I_D=30A	---	155	---	nC
Q_{gs}	Gate-Source Charge		---	36	---	
Q_{gd}	Gate-Drain Charge		---	57	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=250V ID=30A,R_G=25Ω	---	68	---	ns
T_r	Rise Time		---	142	---	
$T_{d(off)}$	Turn-Off Delay Time		---	210	---	
T_f	Fall Time		---	98	---	
C_{iss}	Input Capacitance	V_{DS}=50V , V_{GS}=0V , F=1MHz	---	7860	---	pF
C_{oss}	Output Capacitance		---	755	---	
C_{rss}	Reverse Transfer Capacitance		---	33	---	

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	---	---	50	A
I_{SM}	Pulsed Source Current		---	---	110	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.5	V

Note :

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics (Curves)

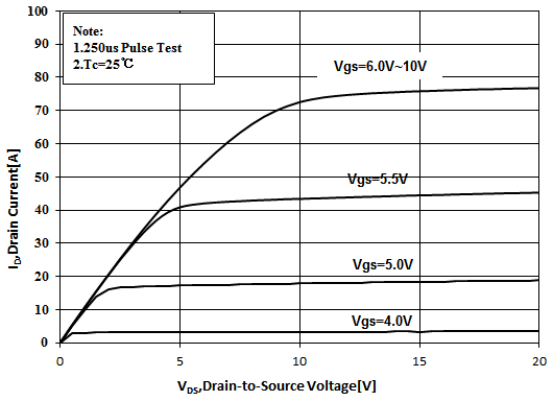


Fig 1: On-Region Characteristics

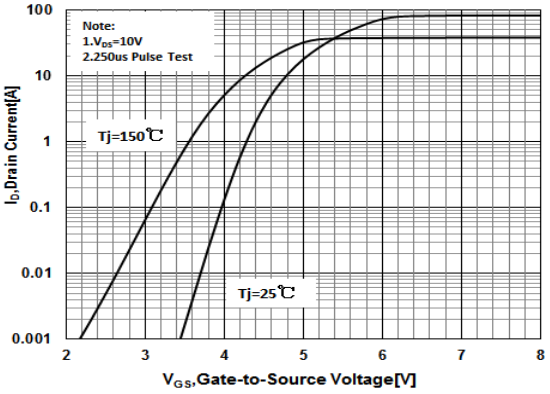


Figure 2: Transfer Characteristics

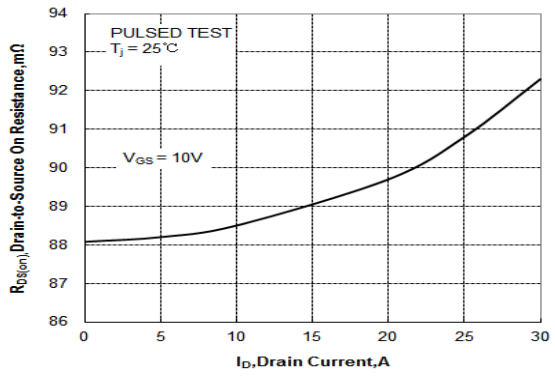


Figure3:On-Resistance vs. Drain Curent and Gate Voltage

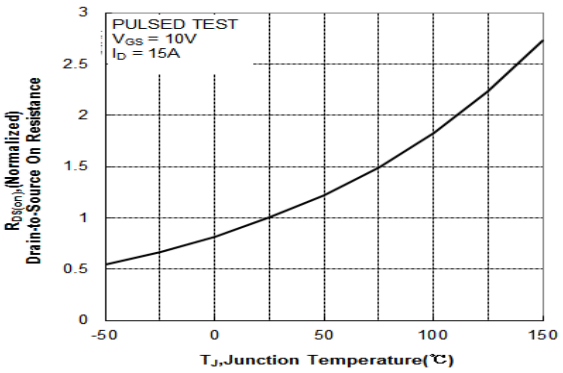


Figure 4:On-Resistance vs.Junction Temperature

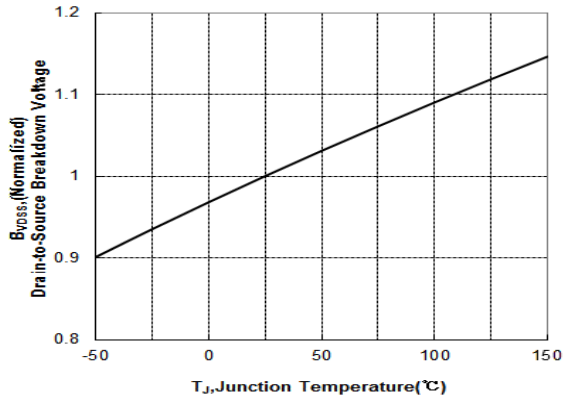


Figure 5: Typical Breakdown Voltage vs Junction Temperature

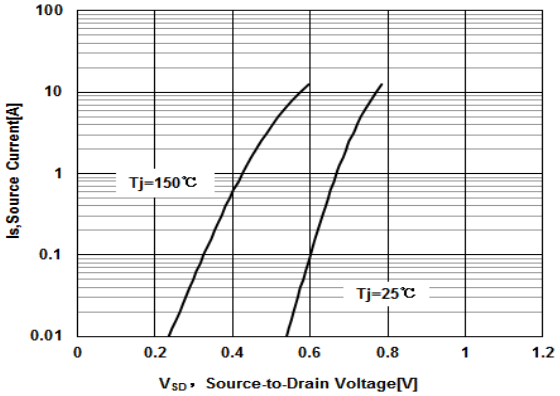


Figure 6: Body-Diode Characteristics

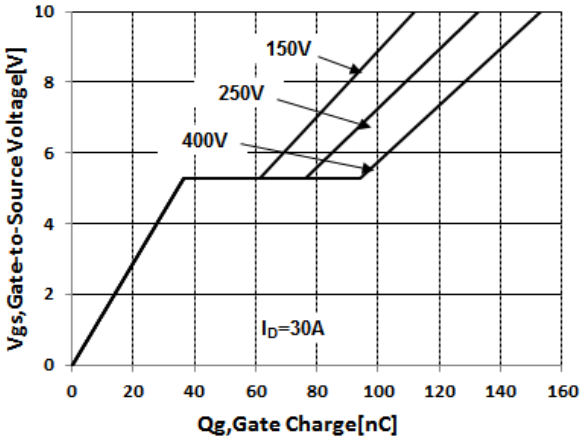


Figure 7: Gate-Charge Characteristics

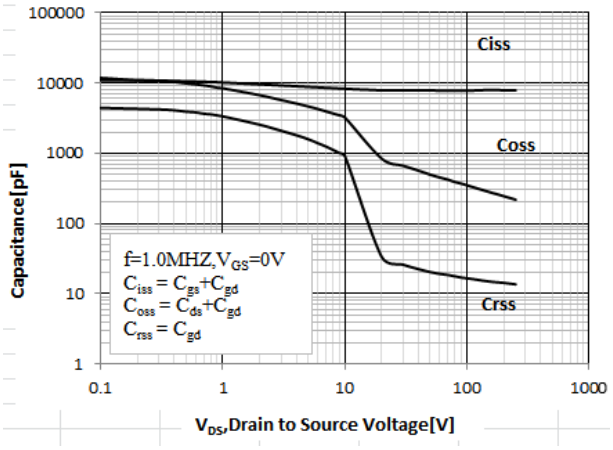


Figure 8: Capacitance Characteristics

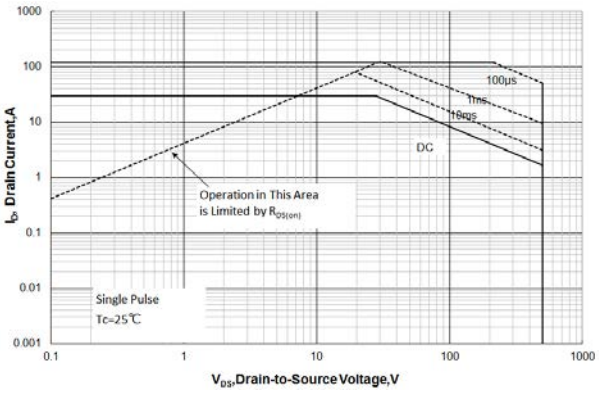


Figure 9: Maximum Forward Biased Safe Operating Area

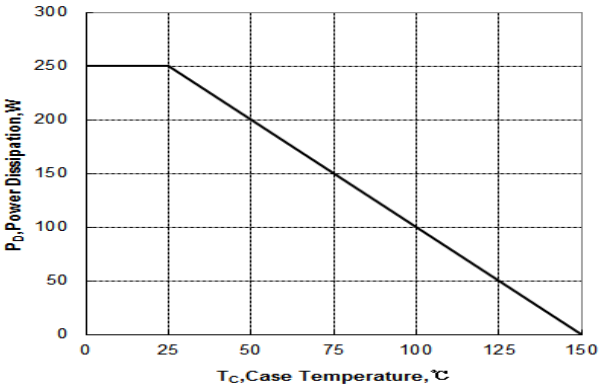


Figure 10: Maximum Power dissipation vs Case Temperature

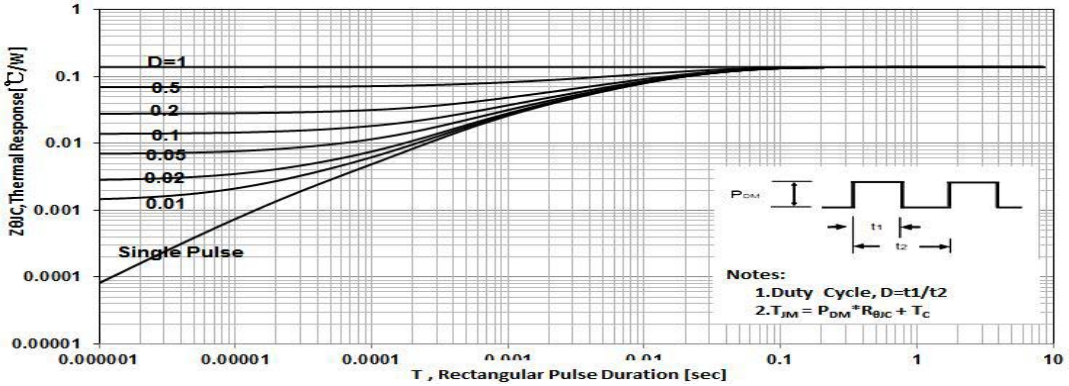


Figure 11: Maximum Effective Thermal Impedance , Junction to Case

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